PALM INTRANET

Inventor Name Search Result

Your Search was:

Last Name = BRUNN
First Name = BRIAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60298633	Not Issued	159	06/15/2001	Radio frequency data conveyance system including configurable integrated circuits	BRUNN, BRIAN
60888183	Not Issued	20	02/05/2007	Frequency and Q Tunable RF Filters	BRUNN, BRIAN
60893462	Not Issued	20	03/07/2007	Frequency and Q Tunable RF Filters Utilizing the Frequency Translatable Impedance (FTI) Structure	BRUNN, BRIAN
60893753	Not Issued	20	03/08/2007	Frequency and Q Tunable RF Filters Utilizing the Frequency Translatable Impedance (FTI) Structure	BRUNN, BRIAN
60893776	Not Issued	20	03/08/2007	Tunable High-Q Transconductor for Bandpass RF Circuits	BRUNN, BRIAN
60908265	Not Issued	19	01/01/0001	Energy Dissipating Filters with Tunable Center Frequencies and Q-Factors	BRUNN, BRIAN
60910861	Not Issued	20	04/10/2007	Energy Dissipating Filters with Tunable Center Frequencies and Q-Factors	BRUNN, BRIAN
09491538	6417729	150	01/26/2000	Linear power control loop	BRUNN, BRIAN T.
09927146	6501339	150	08/10/2001	RING OSCILLATORS WITH IMPROVED SIGNAL-PATH MATCHING FOR HIGH-SPEED DATA COMMUNICATIONS	BRUNN, BRIAN T.
10051222	7058120	150	01/18/2002	INTEGRATED HIGH-SPEED SERIAL-TO-PARALLEL AND PARALLEL-TO-SERIAL TRANSCEIVER	BRUNN, BRIAN T.
10155301	6912698	150	05/23/2002	SKEW LOTS FOR IC OSCILLATORS AND OTHER ANALOG CIRCUITS	BRUNN, BRIAN T.
10243411	7184466	150	09/12/2002	RADIO FREQUENCY DATA CONVEYANCE SYSTEM INCLUDING CONFIGURABLE INTEGRATED CIRCUITS	BRUNN, BRIAN T.
10346435	6977959	150	01/17/2003	CLOCK AND DATA RECOVERY PHASE-LOCKED LOOP	BRUNN, BRIAN T.
10421248	7142622	150	04/22/2003	MULTIPLYING PHASE DETECTOR FOR USE IN A RANDOM DATA LOCKED LOOP ARCHITECTURE	BRUNN, BRIAN T.
10421512	Not Issued	95	04/22/2003	HIGH-SPEED WIDE BANDWIDTH DATA DETECTION CIRCUIT	BRUNN, BRIAN T.
10660235	7092689	150	09/11/2003	CHARGE PUMP HAVING SAMPLING POINT ADJUSTMENT	BRUNN, BRIAN T.
10737386	Not Issued	30	12/16/2003	Adaptive transition density data triggered PLL (phase locked loop)	BRUNN, BRIAN T.
10791924	Not Issued	30	03/02/2004	Bit-edge zero forcing equalizer	BRUNN, BRIAN T.
10900945	7091773	150	07/28/2004	LIMITING CIRCUIT WITH LEVEL LIMITED FEEDBACK	BRUNN, BRIAN T.
10919759	Not Issued	30	08/17/2004	Selective signal coupling in high speed I/O circuits	BRUNN, BRIAN T.

10955062	Not Issued	30	09/29/2004	Differential signal strength detector	BRUNN, BRIAN T.
10997159	Not Issued	30	11/24/2004	Combined decision feedback equalization and linear equalization	BRUNN, BRIAN T.
11095812	Not Issued	30	03/31/2005	Method and apparatus for reducing parasitic capacitance	BRUNN, BRIAN T.
11099865	Not Issued	30	04/05/2005	NRZ/PAM-4/PRML triple mode phase and data detector	BRUNN, BRIAN T.
11111135	Not Issued	30	04/21/2005	Skew lots for IC oscillators and other analog circuits	BRUNN, BRIAN T.
11483009	Not Issued	95	07/06/2006	CHARGE PUMP HAVING SAMPLING POINT ADJUSTMENT	BRUNN, BRIAN T.
09261452	6333975	150	03/03/1999	METHOD AND SYSTEM FOR READING INTELLIGENT UTILITY METERS	BRUNN, BRIAN T.
60076629	Not Issued	159	03/03/1998	COMMERCIAL AND INDUSTRIAL NETWORK	BRUNN, BRIAN T.
09918752	6650195	150	07/30/2001	OSCILLATOR WITH DIFFERENTIAL TUNABLE TANK CIRCUIT	BRUNN, BRIAN TAYLOR

Inventor Search Completed: No Records to Display.

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